

# X1F INTEL SYSTEM DIAGRAM

01

<b>+3V/+5V S5</b>
PG.29
<b>+1.0V</b>
PG.31
<b>CPU Core</b>
PG.33~34
<b>DDR3L</b>
PG.30
<b>Charge</b>
PG.28

<b>SODIMM1</b>	1600MT/s
Max. 8GB	DDR3 L
STD PG.17	Channel A
<b>SODIMM2</b>	1600MT/s
Max. 8GB	DDR3 L
STD PG.18	Channel B

<b>INTEL SkyLake-H</b>
Processor : Daul / Quad Core
Power : 45 (Watt)
Package : BGA1400
Size : 42 x 28 (mm)
PG.2~8

<b>Stackup</b>
TOP
GND
IN1
IN2
VCC
BOT

<b>HDD</b>	PG.26
<b>ODD</b>	PG.26

<b>INTEL PCH Lynx Point</b>
Power : Watt
Package : FCBGA837
Size : 23 x 23 (mm)
PG.9~15

<b>USB 3.0</b>	PORT1, 2
<b>USB3.0 Ports</b>	PG.22; PG.25
<b>USB 2.0</b>	PORT0, 1, 2

<b>Webcam</b>
PG.20

<b>Touch Screen</b>
Elan EKTH3915 for 14", 15"
Elan EKTH3918 for 17"
PG.24

<b>PCI-E x 1</b>
LAN RTL8111GSH 10/100/1000 PG.22
WLAN BT COMBO PG.26

<b>PCI-E x 1</b>
Accelerometer PG.24
Card Reader RTS5237 PG.22

<b>KBC</b>	ITE IT8987E/BX	PG.27
TPM	SLB9656TT1.2	PAGE 24
KB	PG.23	
TP	PG.23	
ROM	PG.12	
FAN	PG.23	
SLG3NB3454	GreenCLK	PAGE 24
25MHz		

The diagram shows a central block labeled **AUDIO CODEC** with the model number **ALC 3241** below it. To the right of this block is a smaller block labeled **He TP**. Below the **AUDIO CODEC** block are two more blocks: **Speaker** on the left and **Dual Digital MIC** on the right. Lines connect the **AUDIO CODEC** block to each of these three blocks. The label **PG.21** is located to the right of the **AUDIO CODEC** block, between its right side and the **Dual Digital MIC** block. Below the **Speaker** and **Dual Digital MIC** blocks are the labels **PAGE 21**.

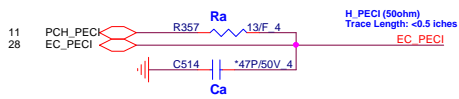
Headphone amplifier TPA6133A2 03 PAGE 22	Hp MIC	Combo Jack PAGE 21
------------------------------------------------	-----------	-----------------------

# SKYLAKE Processor (CLK,MISC,JTAG)

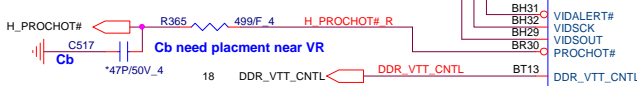
02

Host CLK:  
Trace length < 11000 MILS  
Trace spacing = 15, 20 MILS, Impedance 85 ohm

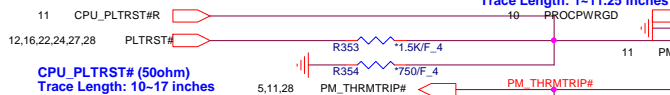
HPECI Ra,Ca need placement close to PCH.



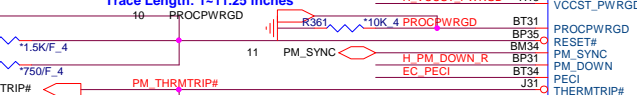
PROCHOT# (50ohm)  
Trace Length <11 inches



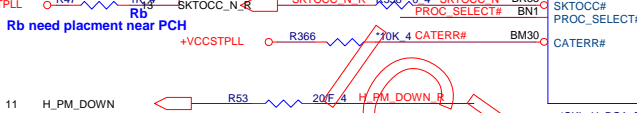
CPU RESET#



PM\_SYNC (50ohm)  
Trace Length: 1-11.25 inches



THERMTRIP# (50ohm)  
Trace Length: 1.1-12 inches



Rb need placement near PCH

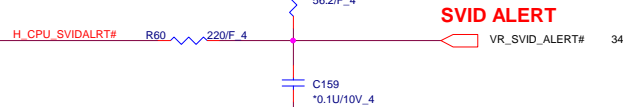


Change R110 from NI 100K to NI 10K and add R527 0ohm PD\_20150128

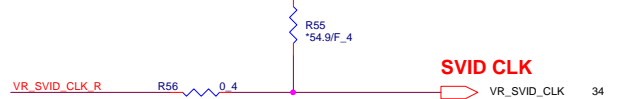
## CPU CORE SVID

Layout note: need routing together and ALERT need between CLK and DATA.

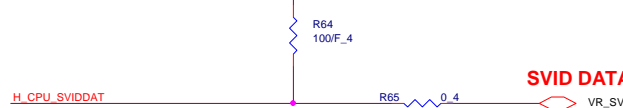
CLOSE TO CPU  
PLACE THE PU RESISTORS



PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



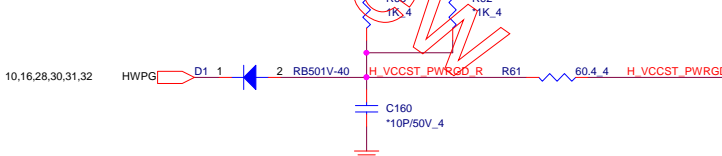
CLOSE TO CPU  
PLACE THE PU RESISTORS



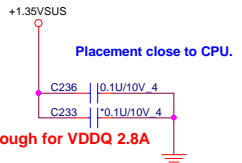
SVID DATA

## HWPDP

R10479 close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"



## CPU VDDQ

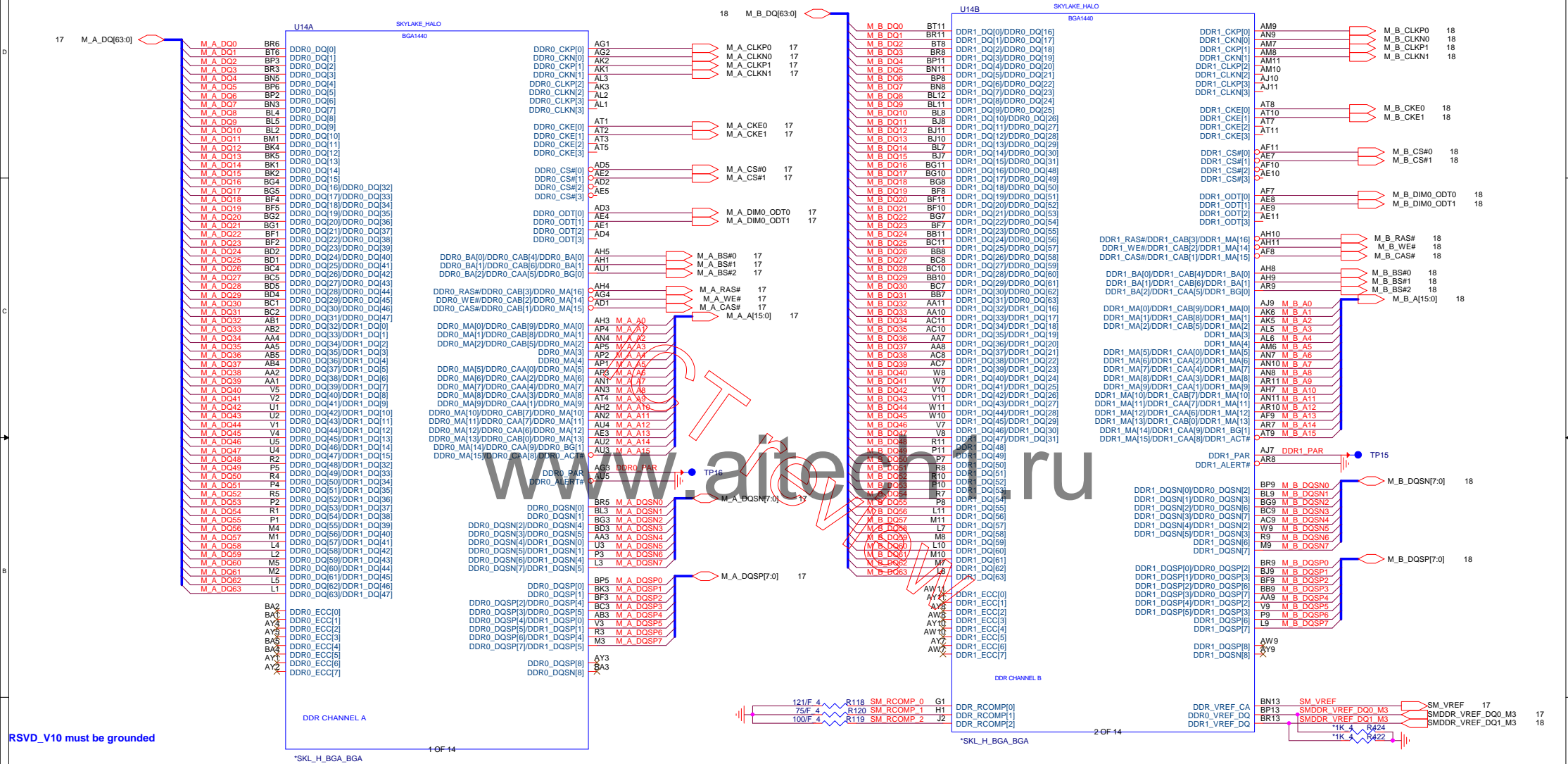


	PROJECT : X1F		
	Quanta Computer Inc.		
	Size Custom	Document Number 02 - SKYPAKE 1/20(eDP/DDI)	Rev 1A
Date: Friday, June 05, 2015	Sheet 2 of 37		



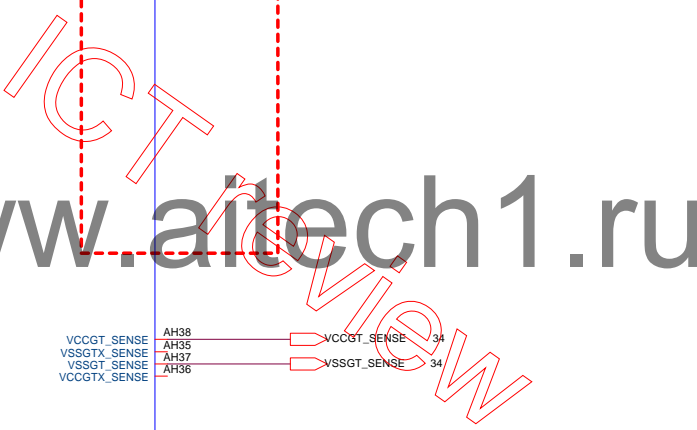
# SKYLAKE Processor (DDR3)

04



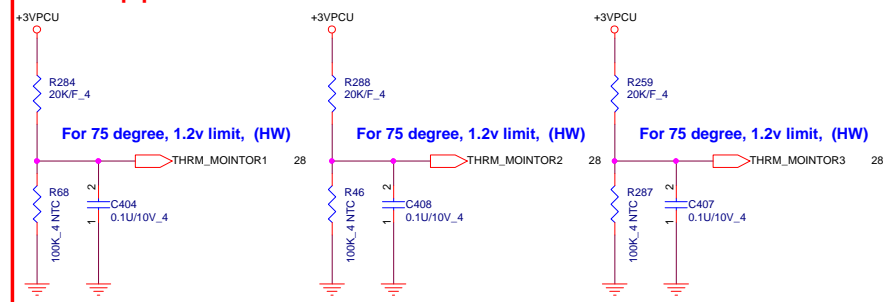
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

4+4e, Support eDRAM Only, GTX 12A

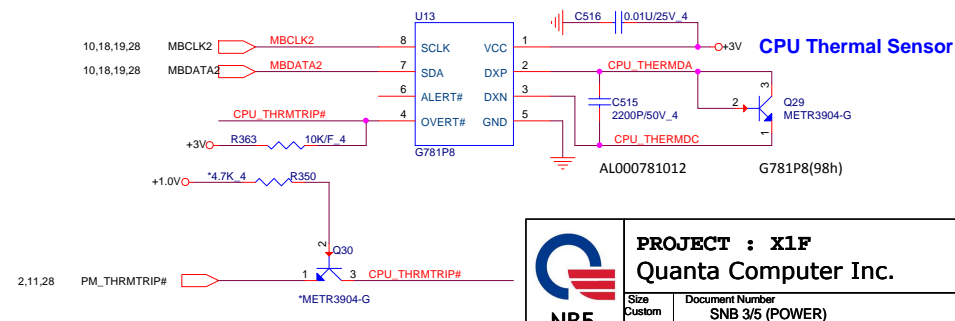


14 OF 14

\*SKL H BGA BGA



### Local Thermal Sensor



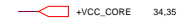
## VCC Output Decoupling Recommendations




**PROJECT : X1F**  
**Quanta Computer Inc.**

Size Custom	Document Number SNB 3/5 (POWER)	Revision 2A
Date: Friday, June 05, 2015	Sheet 5 of 37	

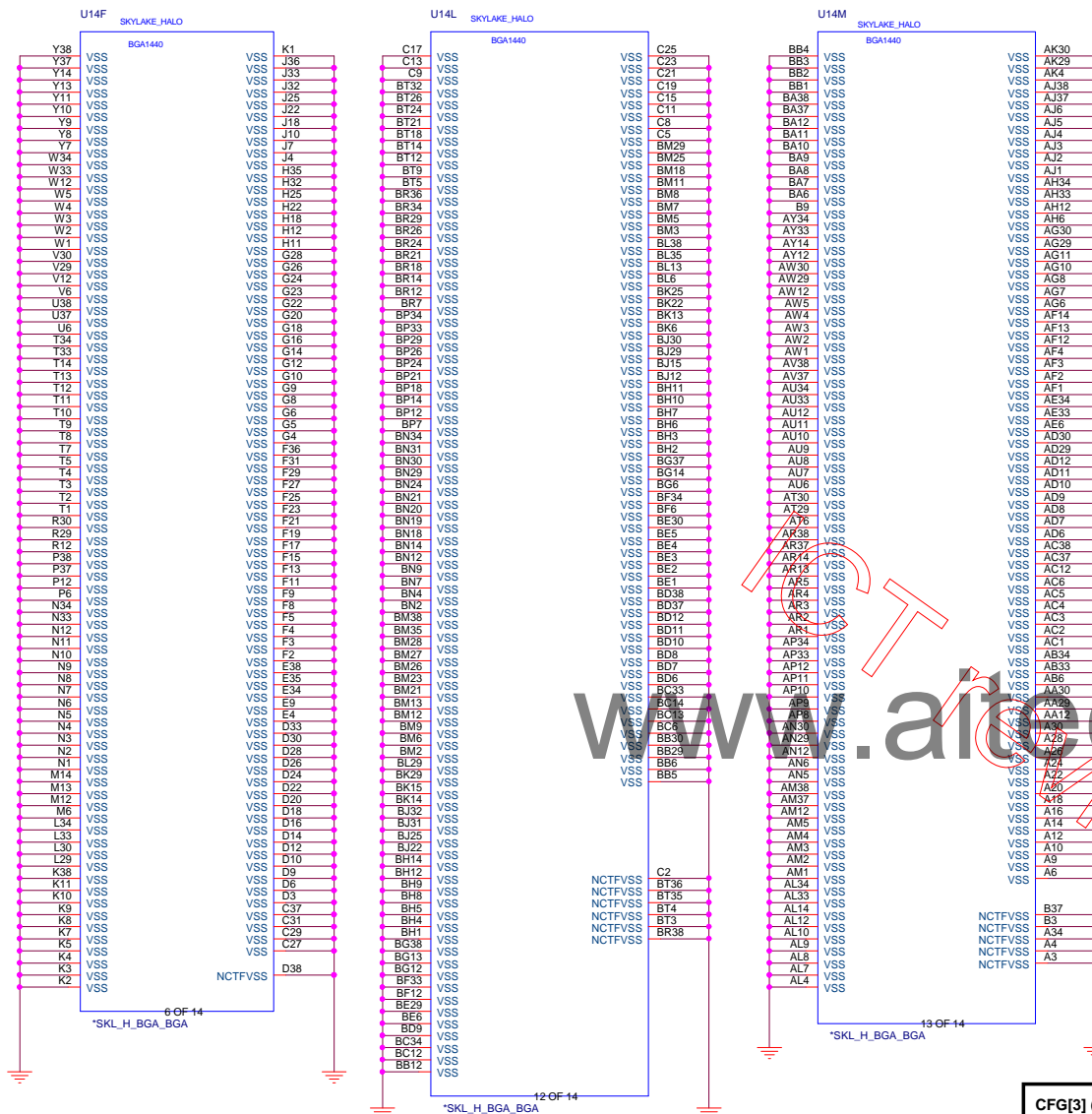




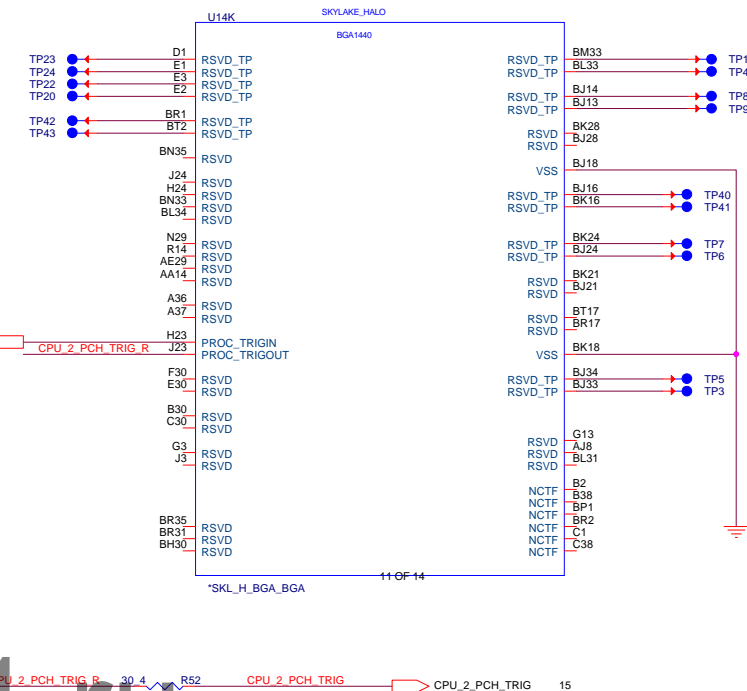
**Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket**  
**Trace Impedance 50 ohm**



Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



## Processor Strapping

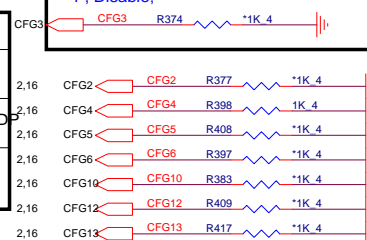
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

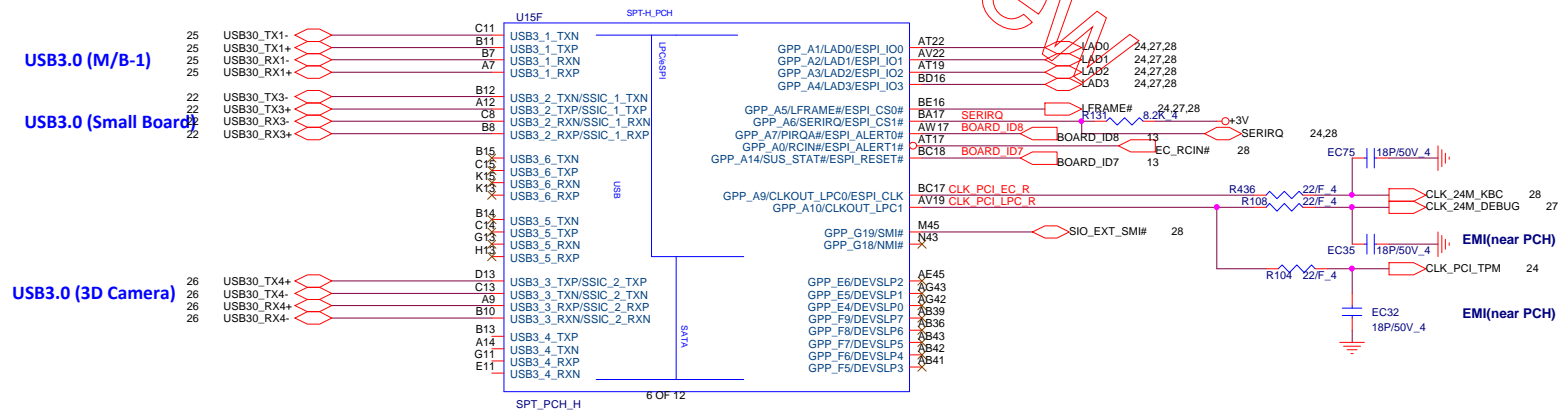
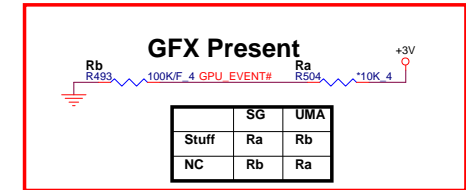
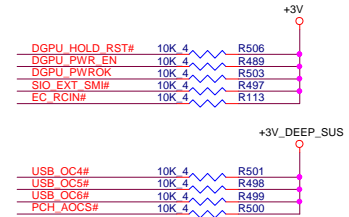
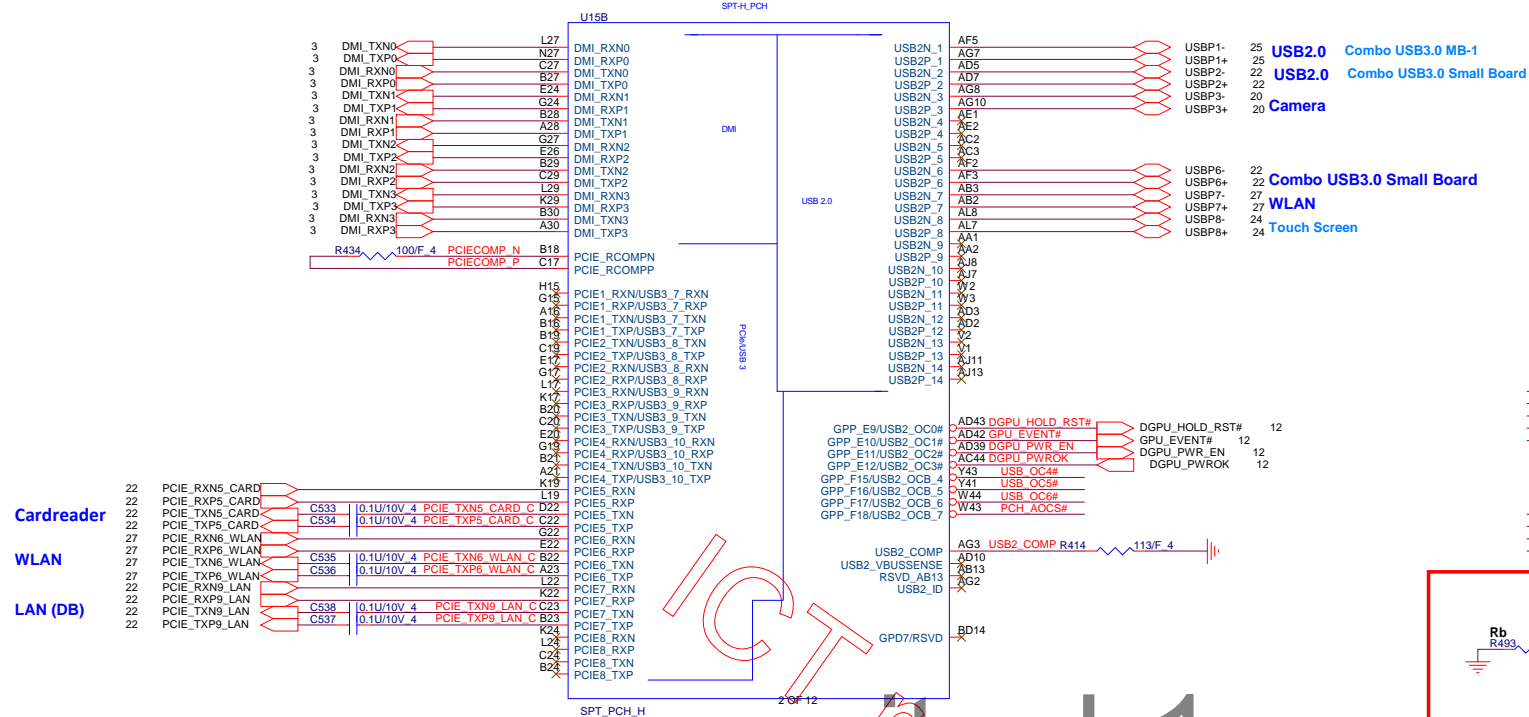
## CFG[3] (PHYSICAL\_DEBUG\_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

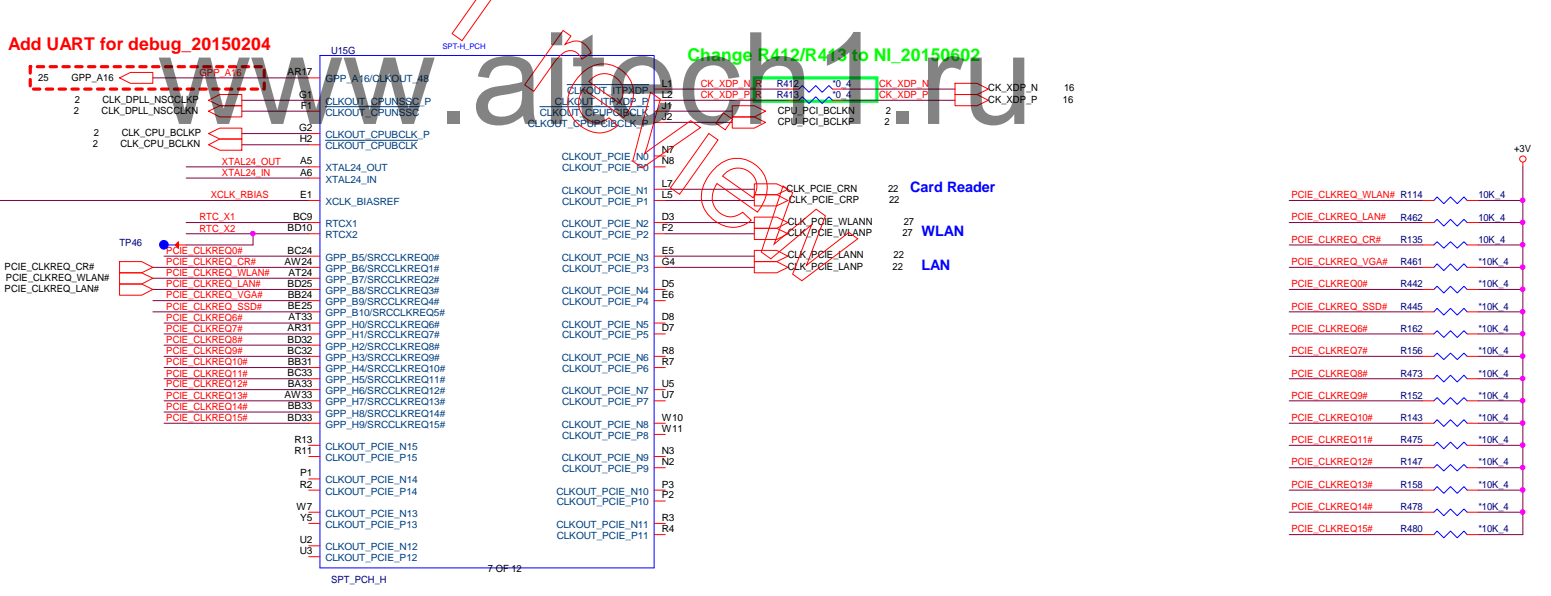
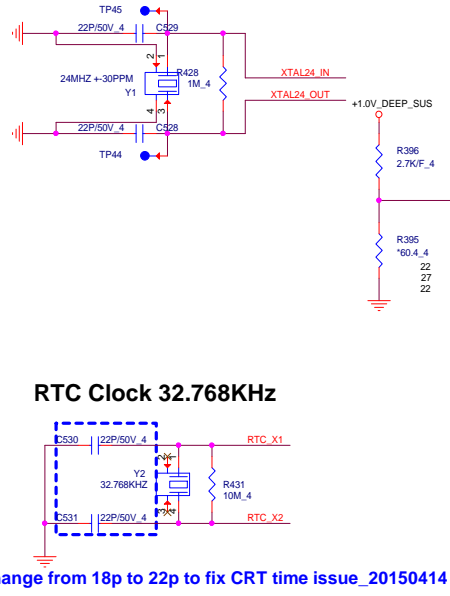




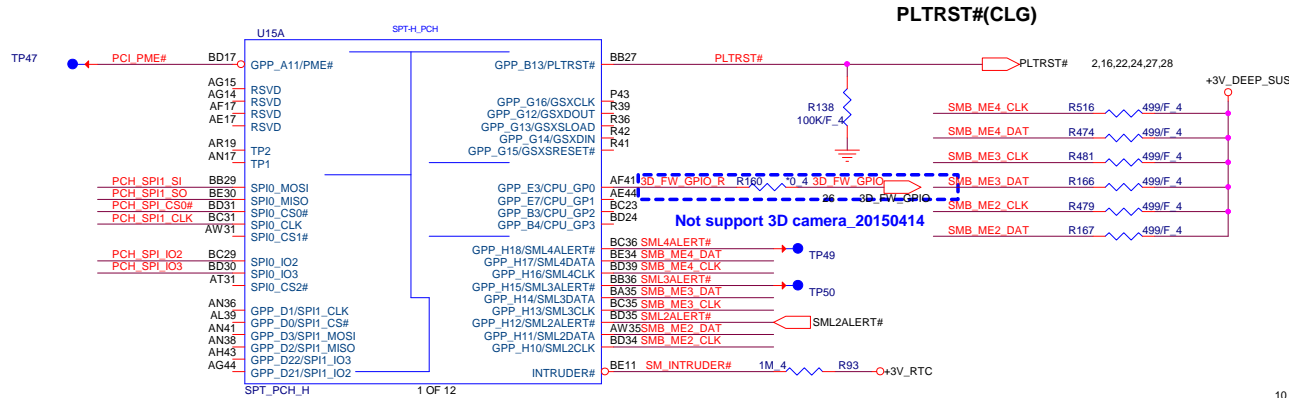


10,12,13,14,16,18 +3V\_DEEP\_SUS





Change from 18p to 22p to fix CRT time issue\_20150414

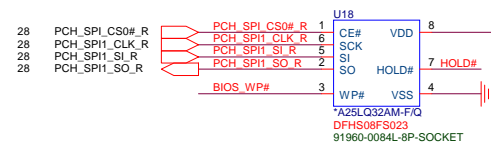


Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP (QE
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGNOQ01 (GD25B64BSIGR)

### PCH SPI ROM(CLG)

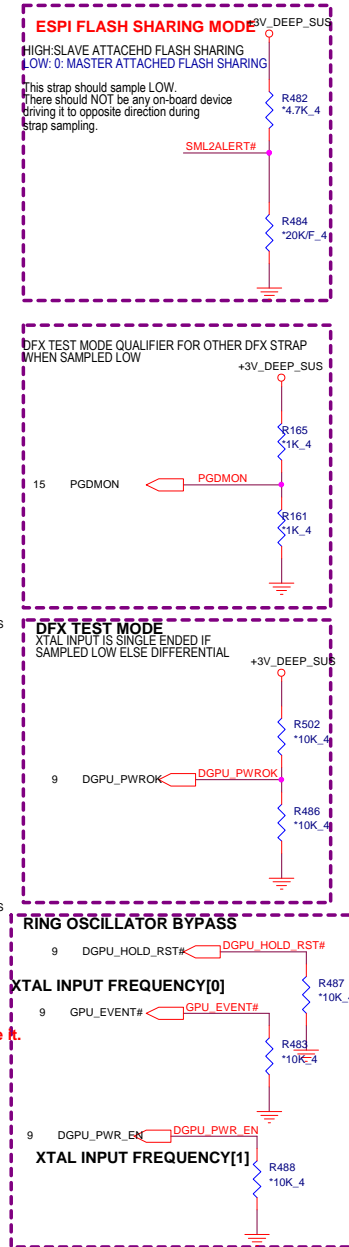
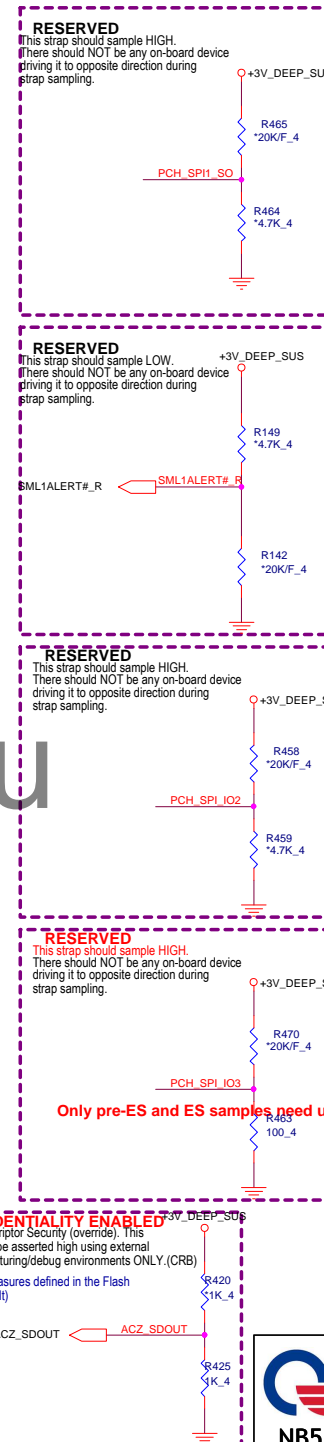
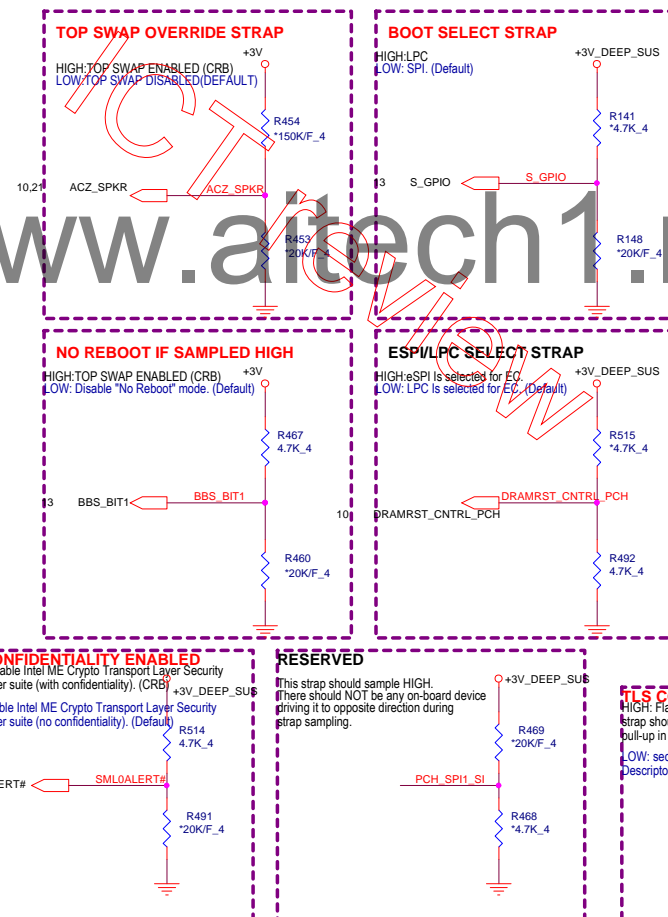
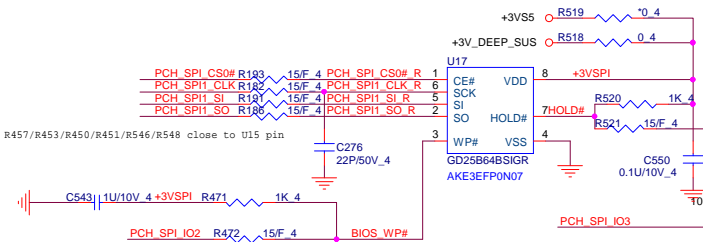
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

### 4M SPI ROM Socket

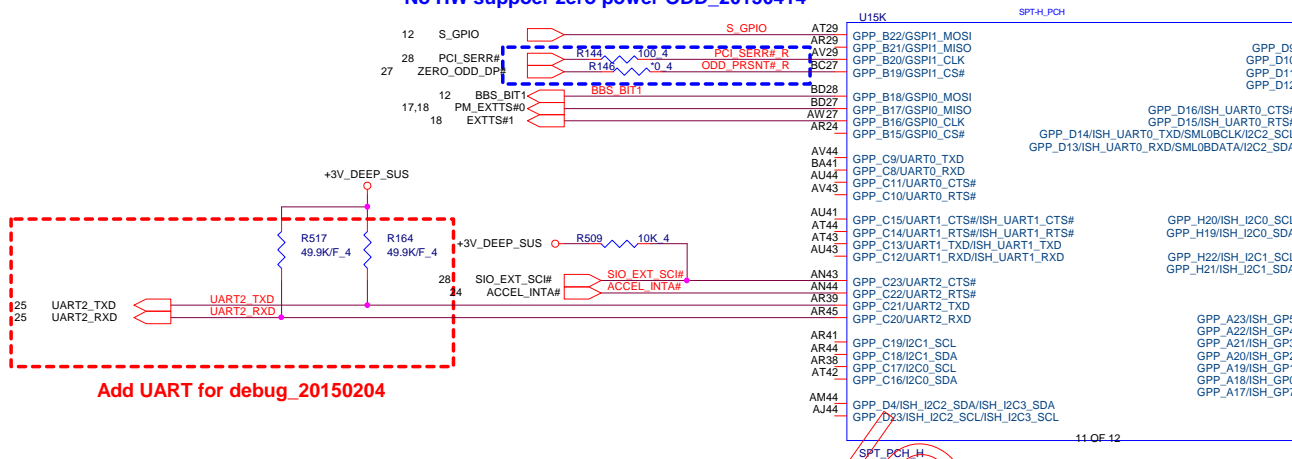


U18&U17 footprint 要重疊

## PCH SPI ROM(CLG)

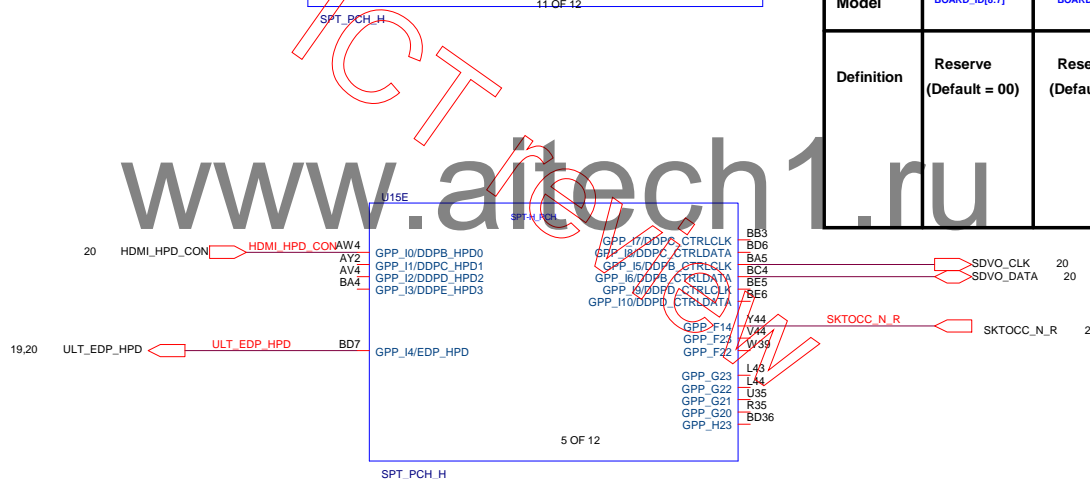
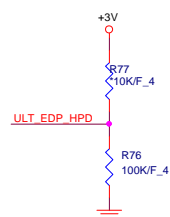


change PCI\_SERR from GPP\_B21 to GPP\_B20\_20150415  
No HW suppoer zero power ODD\_20150414

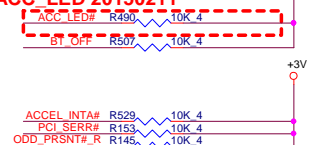


## Add UART for debug\_20150204

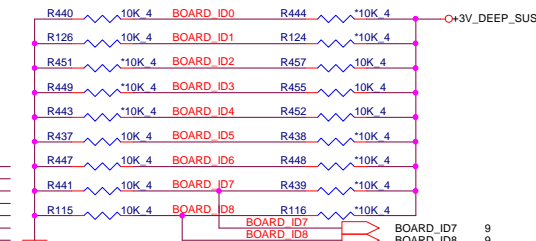
Reserve EDP\_HPD opposites circuit!



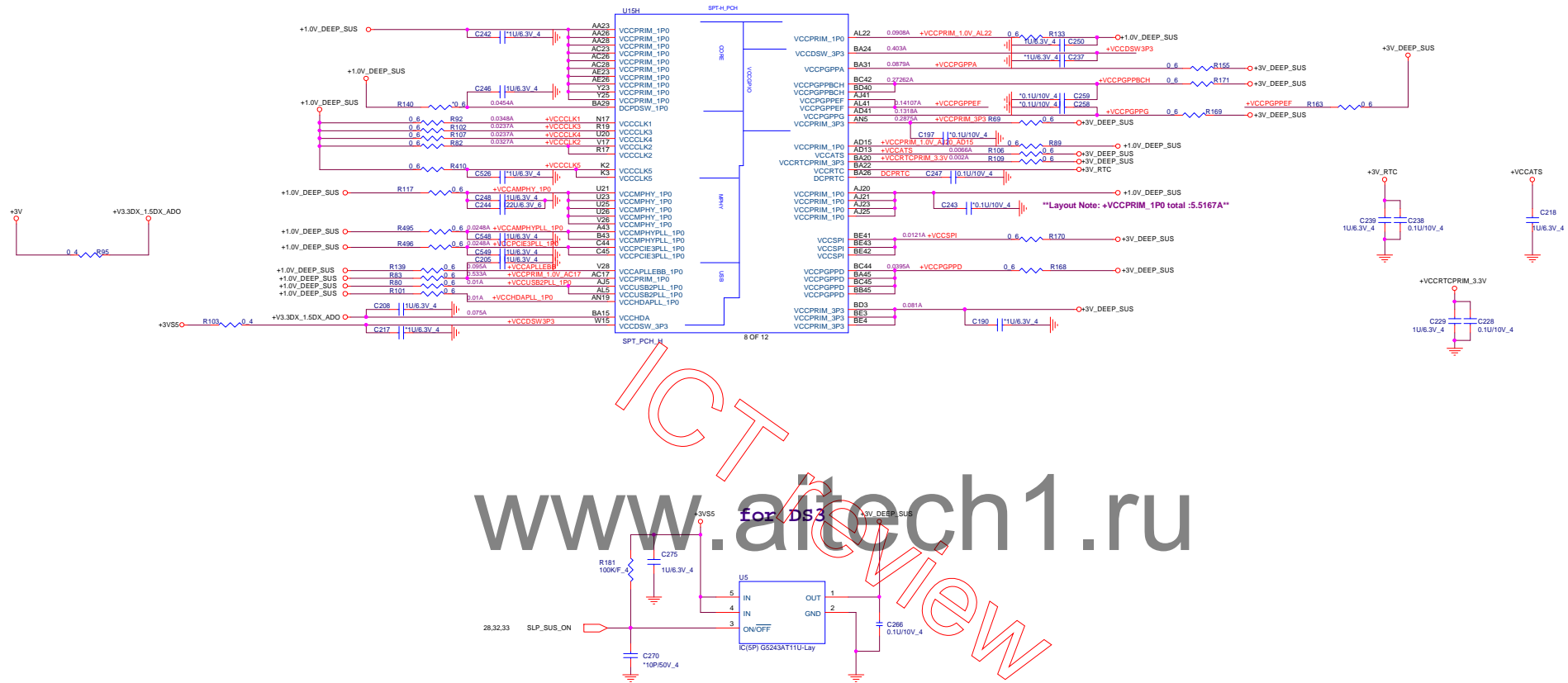
**Add R490 PU +3V\_DEEP\_SUS for ACC\_LED 20150211**



Change R1 to NI for 3D camera\_20150202



Model	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID[0]
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X1B) 01 Dual Rank (X1B) 10 Meso-AMD (X1A) 11 Reserve (X1F)	00 14" 01 15" 10 17"	0 : UMA 1 : DIS

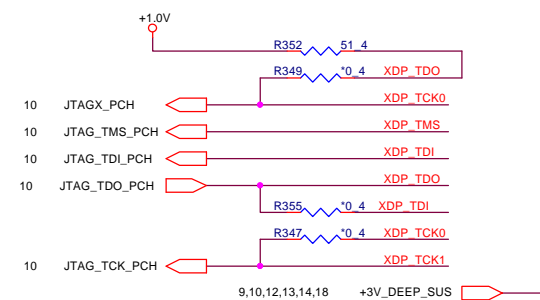
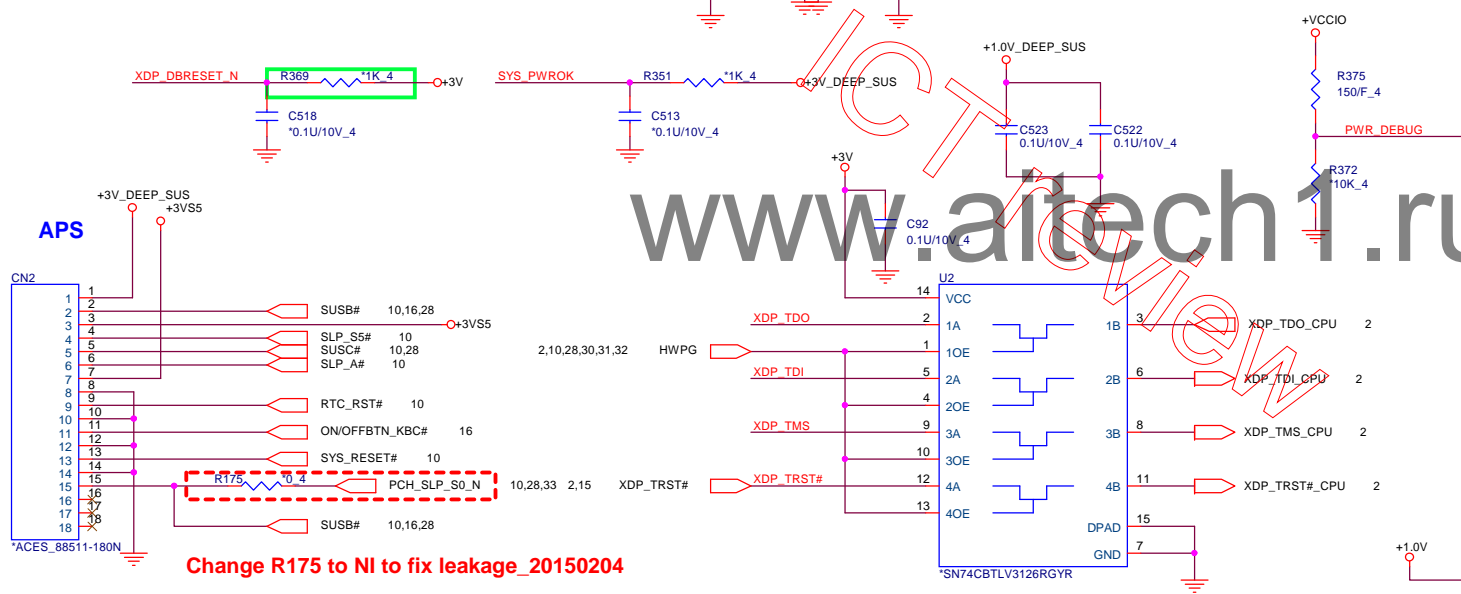
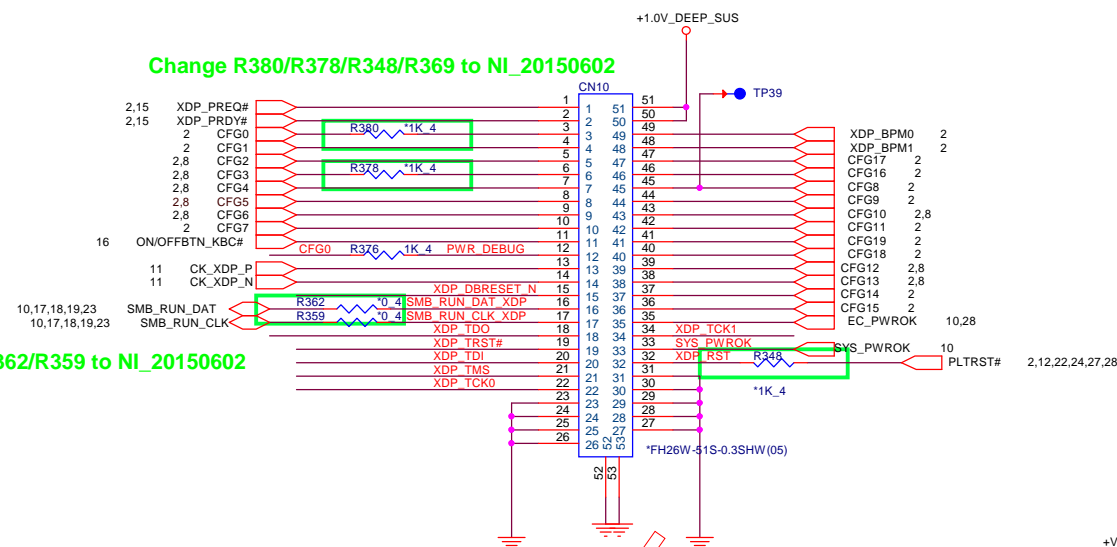


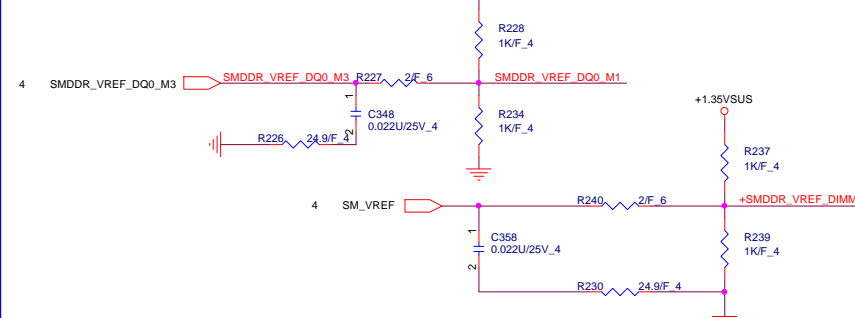
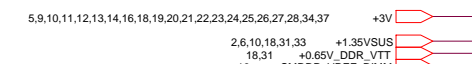
9,10,12,13,16,18 +3V\_DEEP\_SUS 

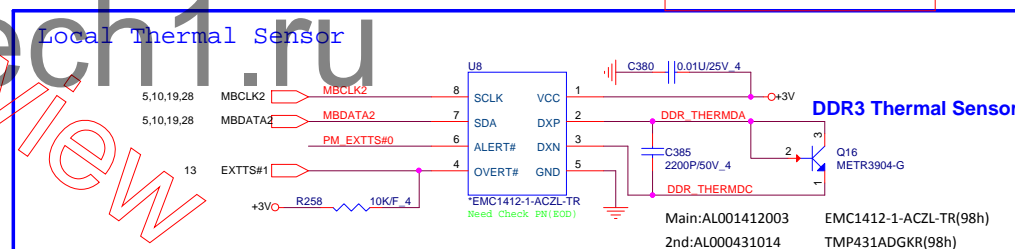
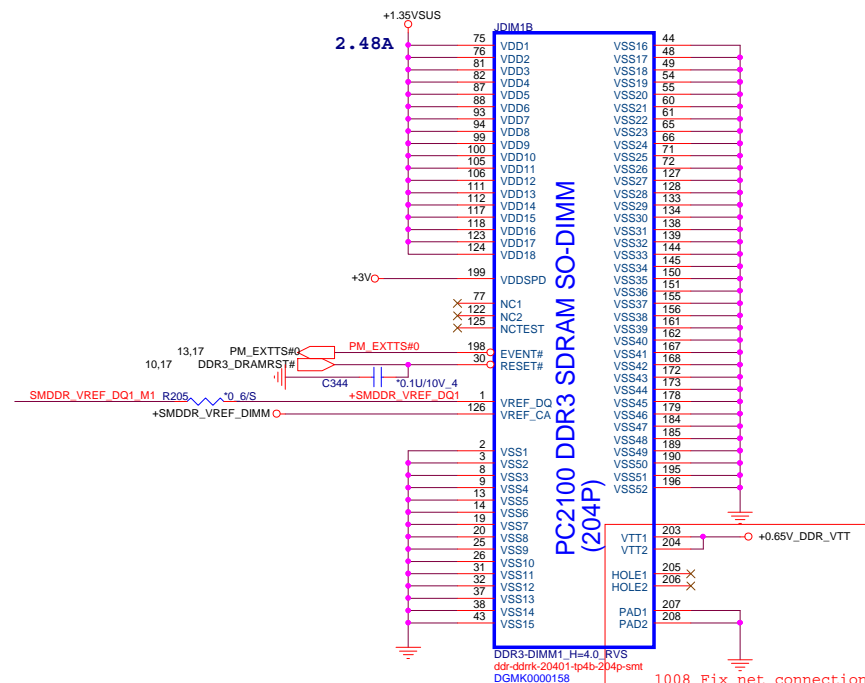




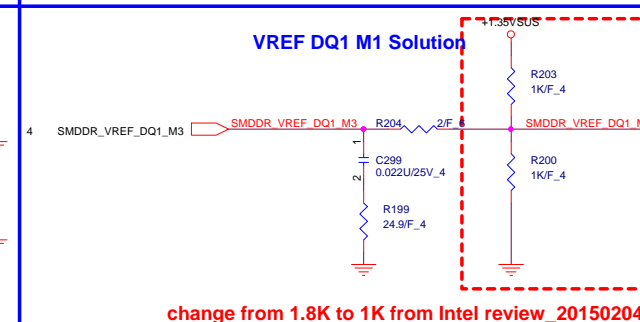
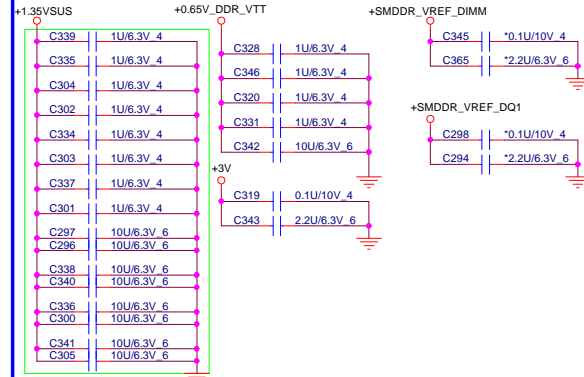




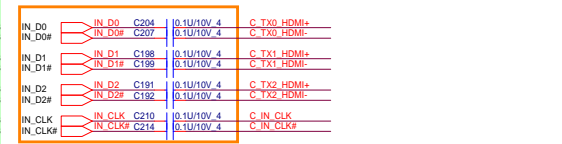
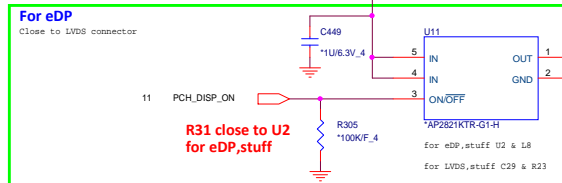
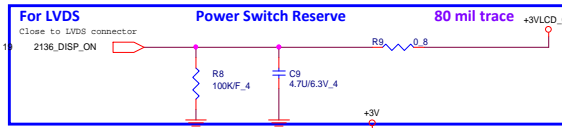
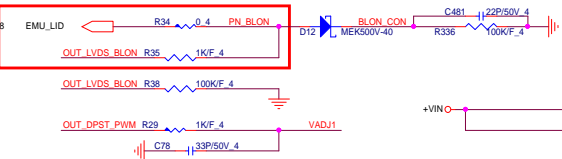


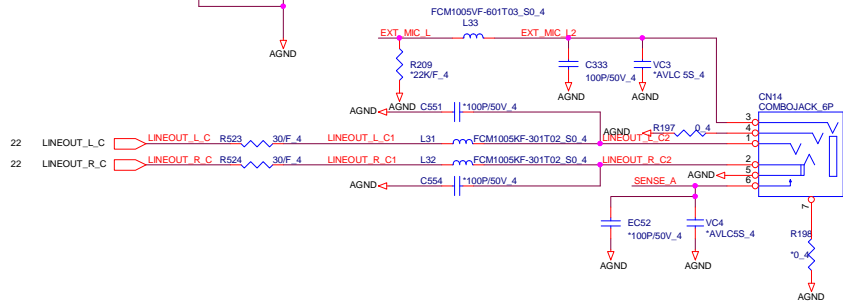
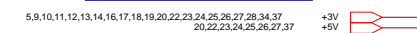
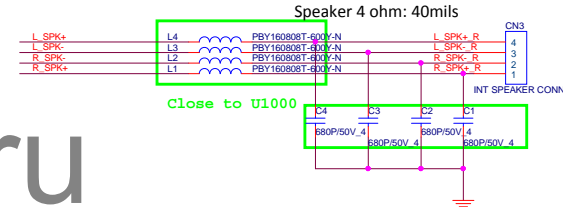
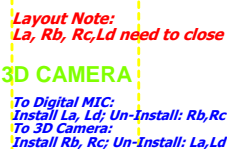
[illegible]

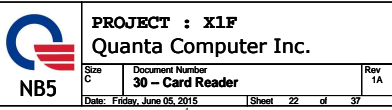
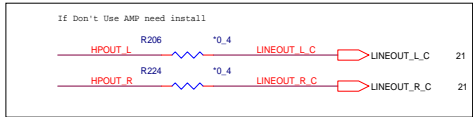
### VREF DQ1 M1 Solution













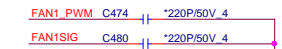


## MUTE\_LED\_CNTL



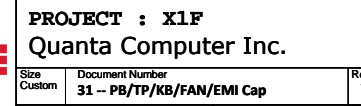
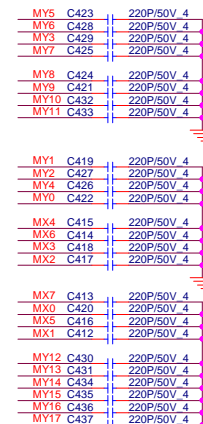
WIRELESS\_ON EC69 | \*220P/50V\_4

WIRELESS\_OFF EC70 | \*220P/50V\_4



WIRELESS\_ON EC69 | \*220P/50V 4

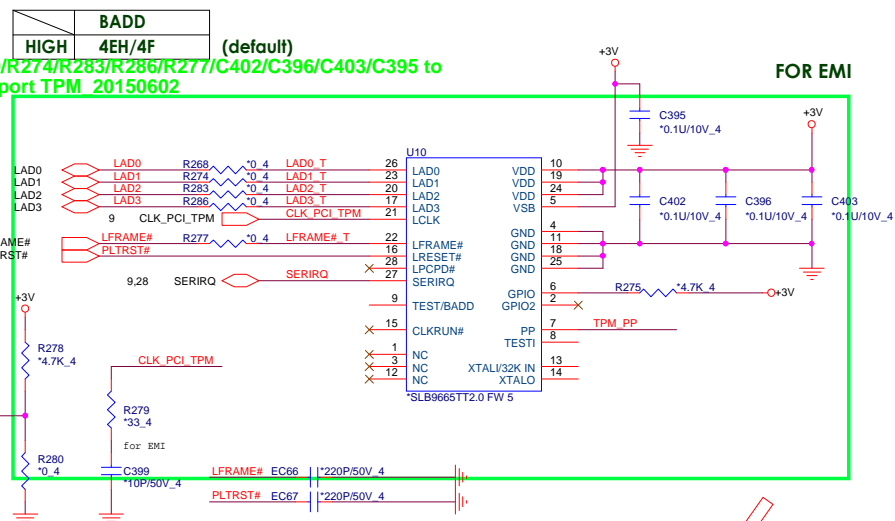
WIRELESS\_OFF EC70 | \*220P/50V 4



## TPM (2.0)

Address

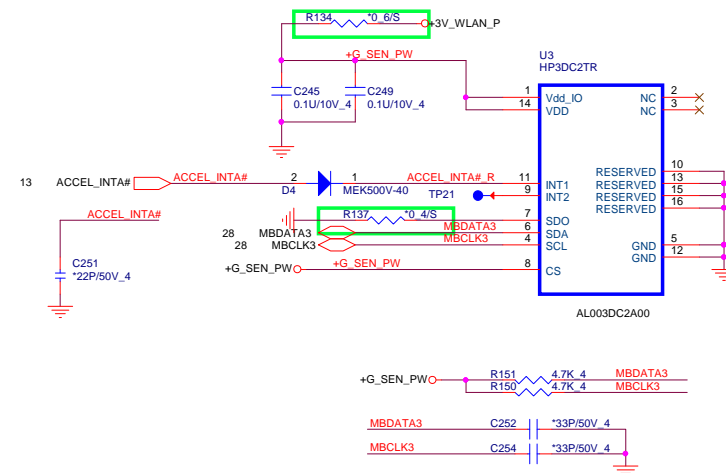
Change  
R268/R280/R274/R283/R286/R277/C402/C396/C403/C395 to  
NI not support TPM 20150602



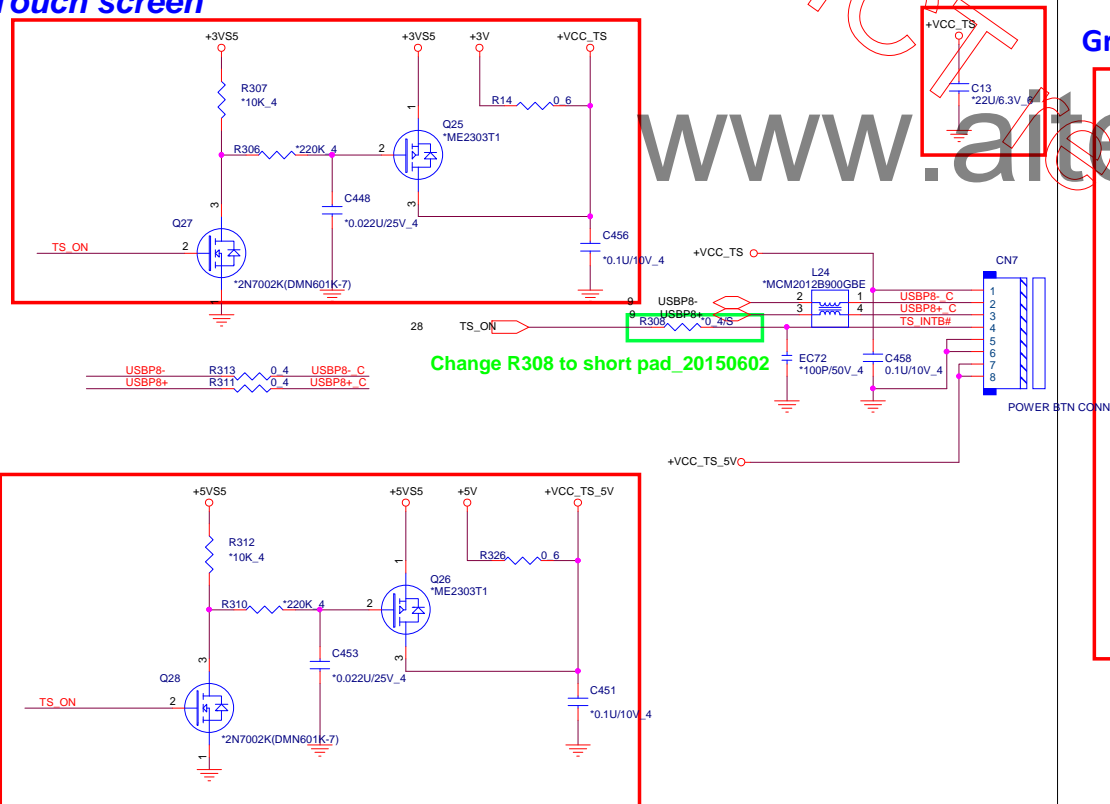
## Accelerometer Sensor

Change R134/R137 to Short pad\_20150602

G-Sensor Power need check



## Touch screen



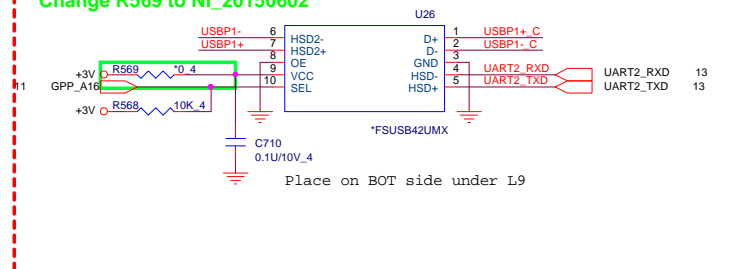
## Green CLK Circuitry



1225 : remove G-CLK function for UMA

## UART for DEBUG

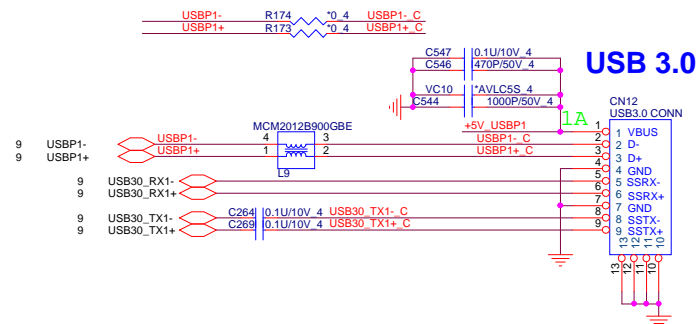
Change R569 to NI\_20150602



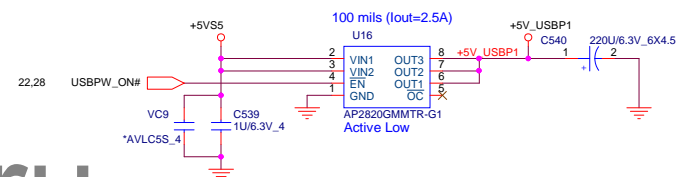
Place on BOT side under L9

Add UART for debug\_20150204

## USB 2.0/3.0 Combo



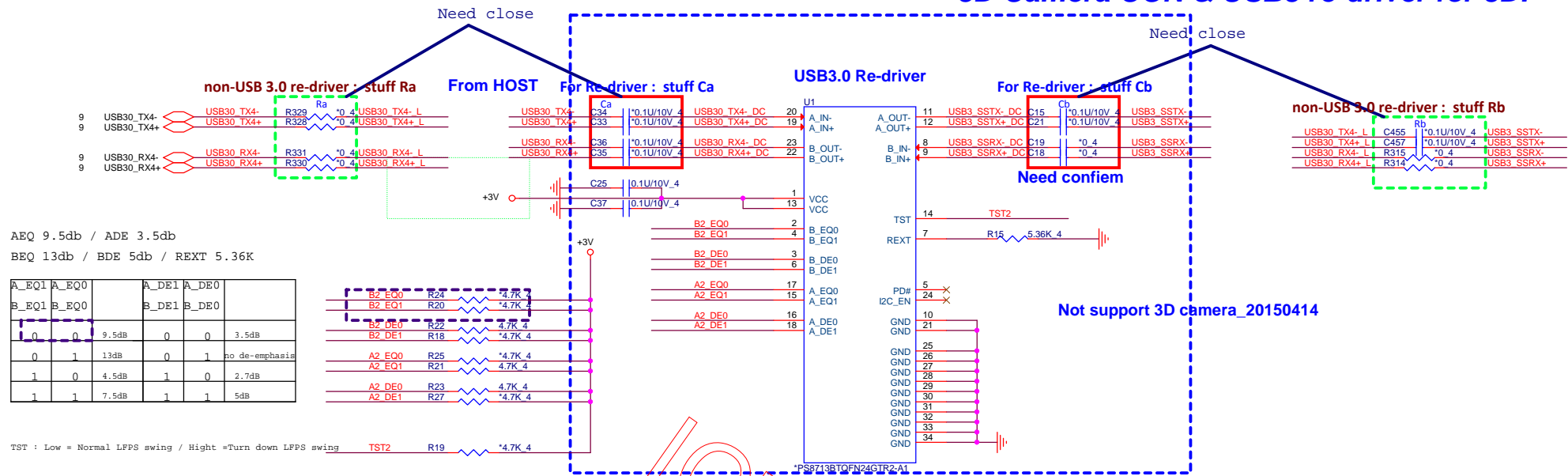
## USB 3.0



www.aitech1.ru

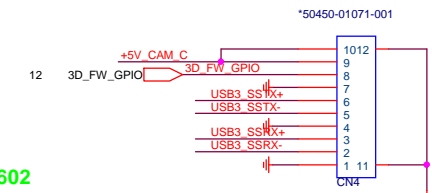
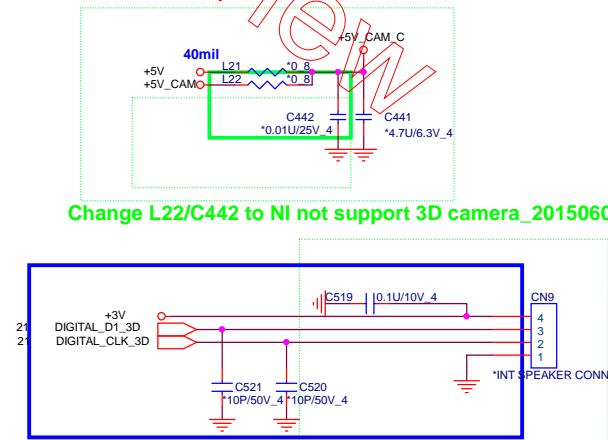
## EMI CAP



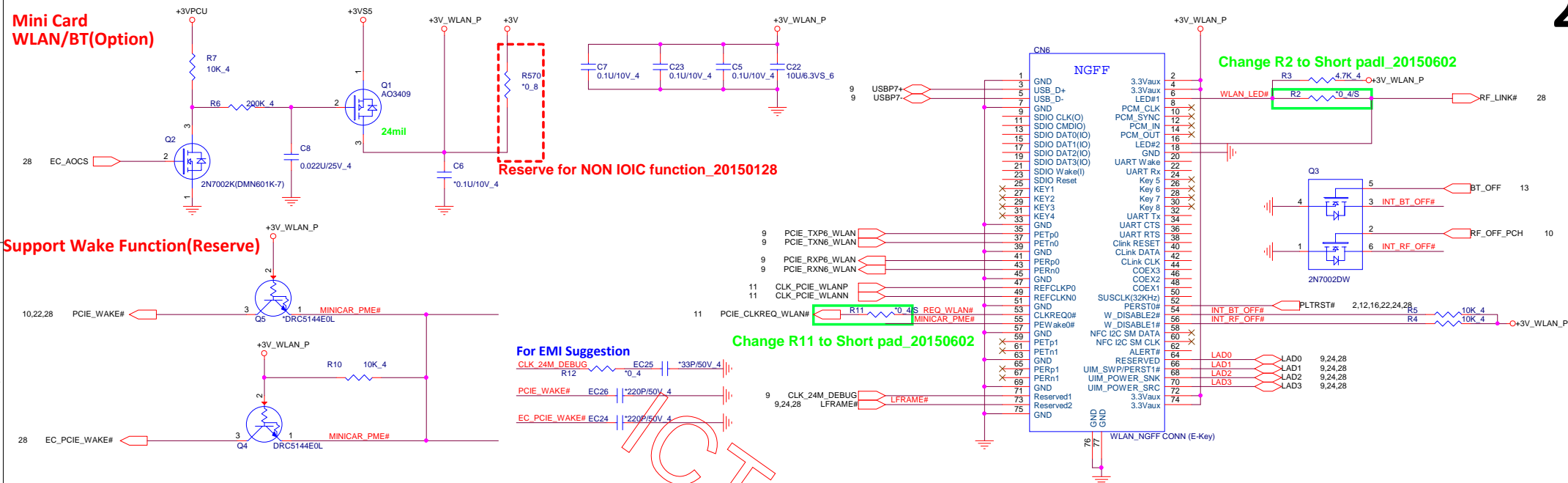


www.aitech1.ru

## 3D Camera Conn.

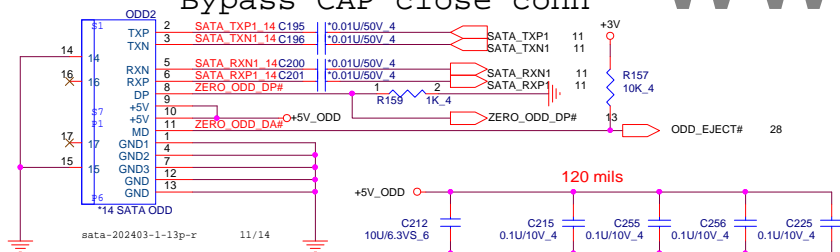


# Mini Card WLAN/BT(Optional)

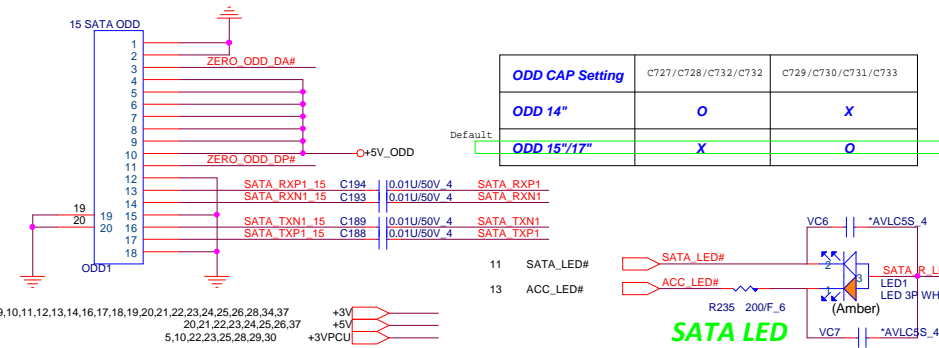


## 14" SATA ODD

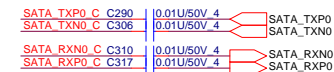
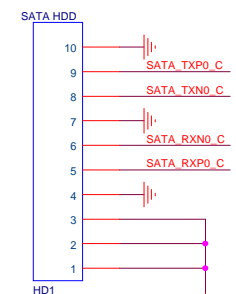
Bypass CAP close conn



## 15" SATA ODD

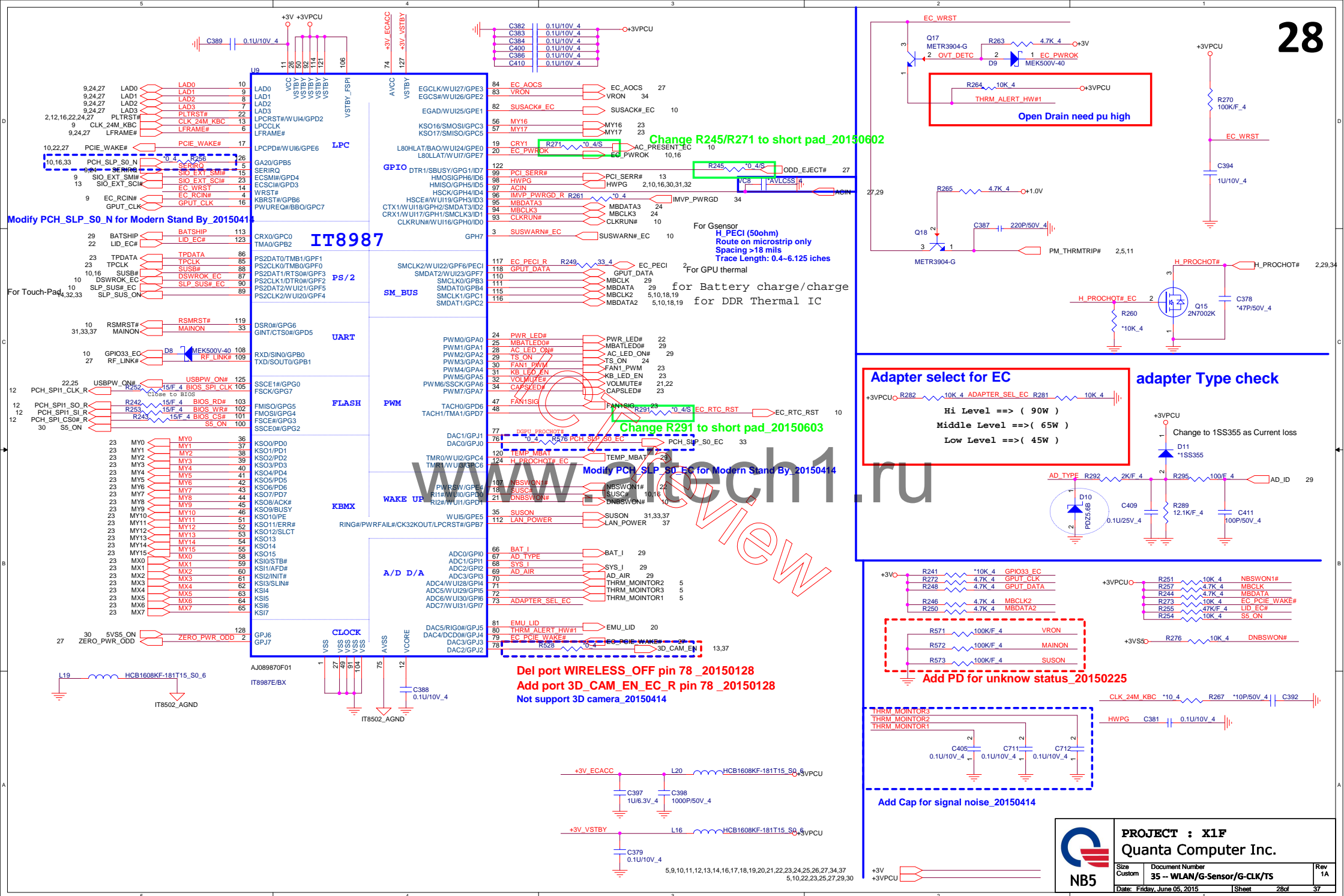


## HDD



PROJECT : X1F  
Quanta Computer Inc.






Size	Document Number	Rev
Custom	34 - WLAN/NGFF/MSATA	1A
Date: Friday, June 05, 2015	Sheet	27 of 37

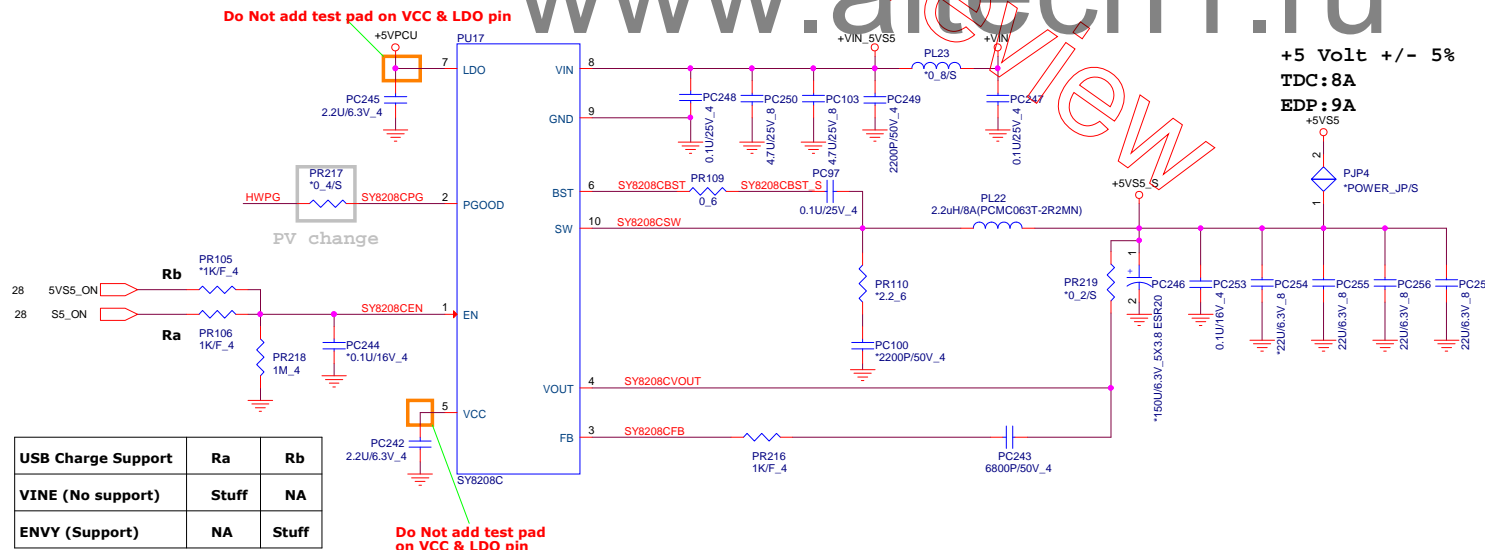
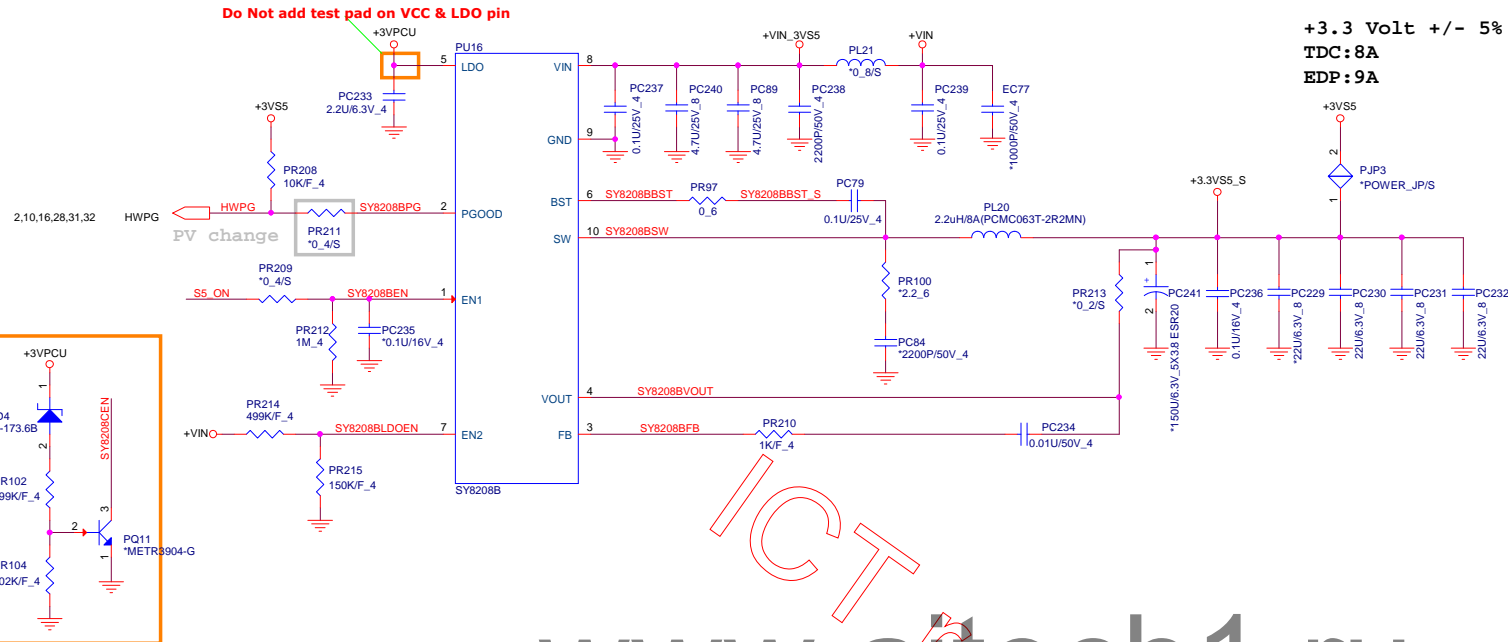




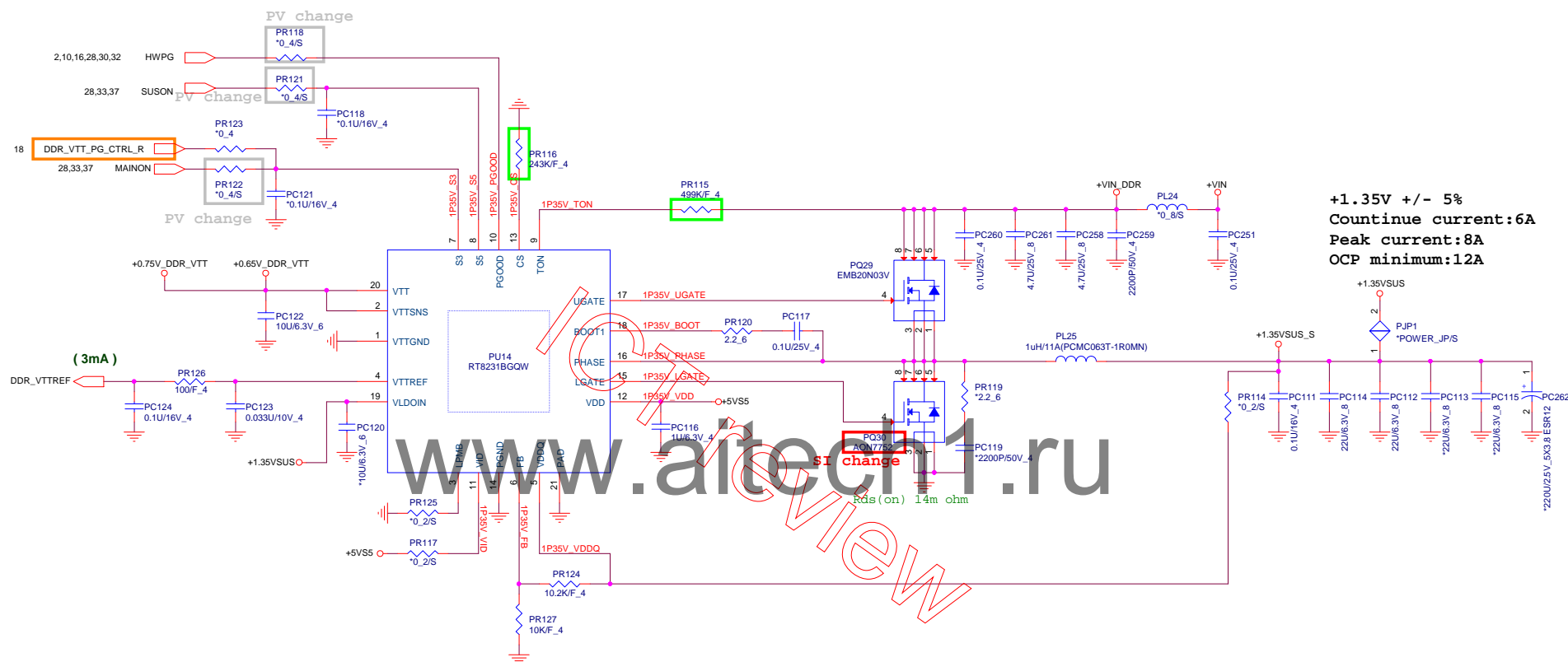


5  
DC/DC +3VS5/+5VS5

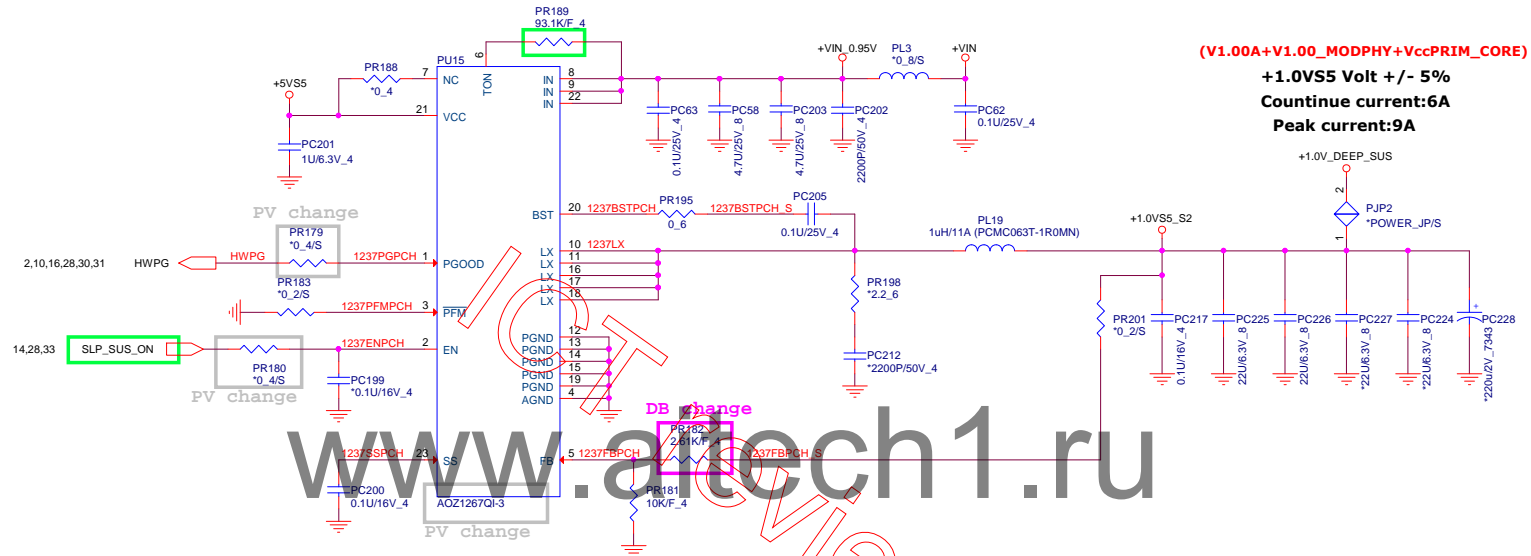
	+VIN	20,23,25,27,29,31,32,34,35,36,37
	+3VS5	10,12,14,16,24,27,28,33,37
	+5VS5	10,22,24,25,31,32,33,34,35,36,37
	+3VPCU	5,10,22,23,25,27,28,29
	+5VPCU	29

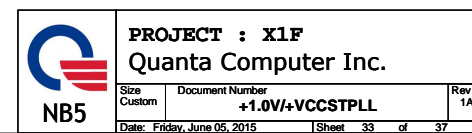


USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

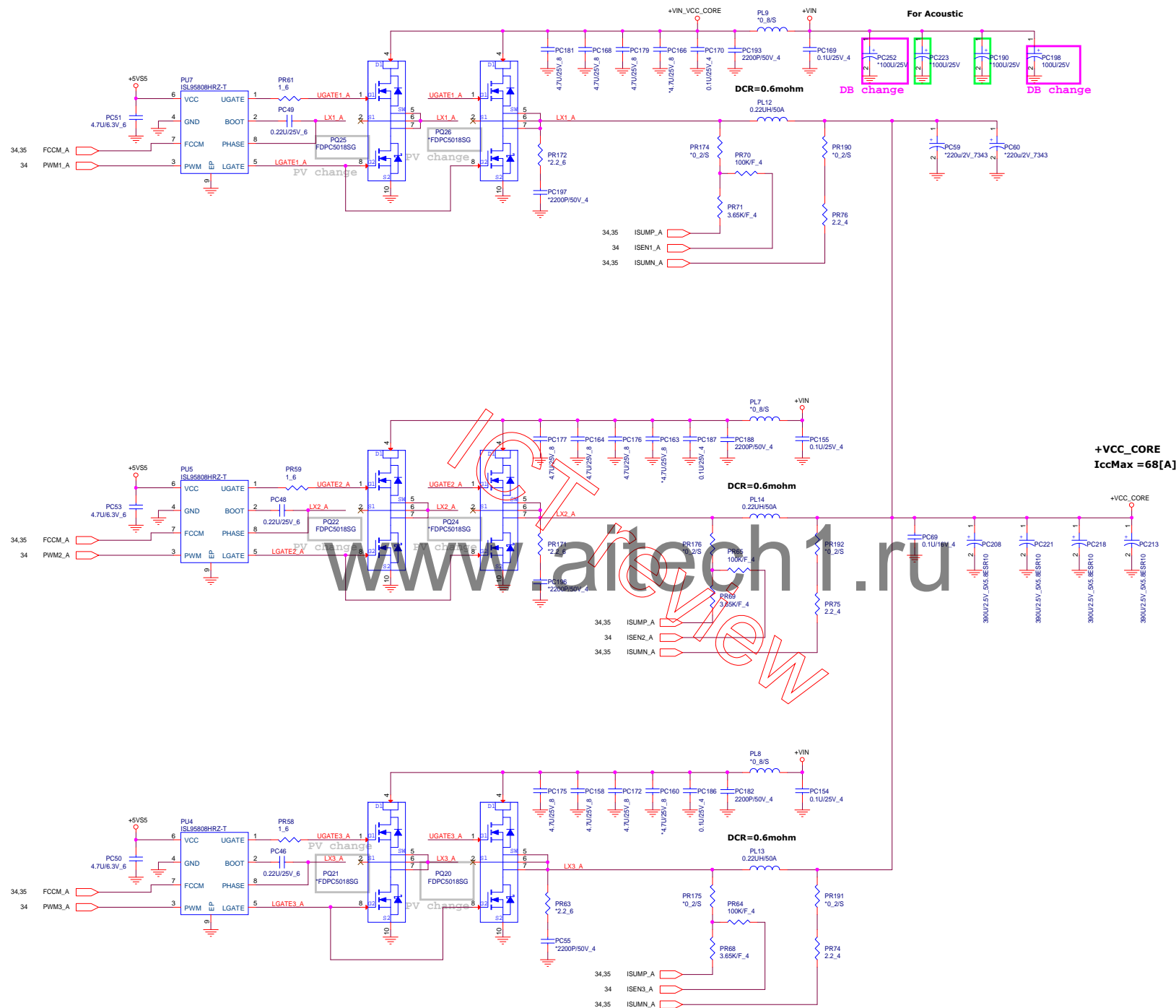


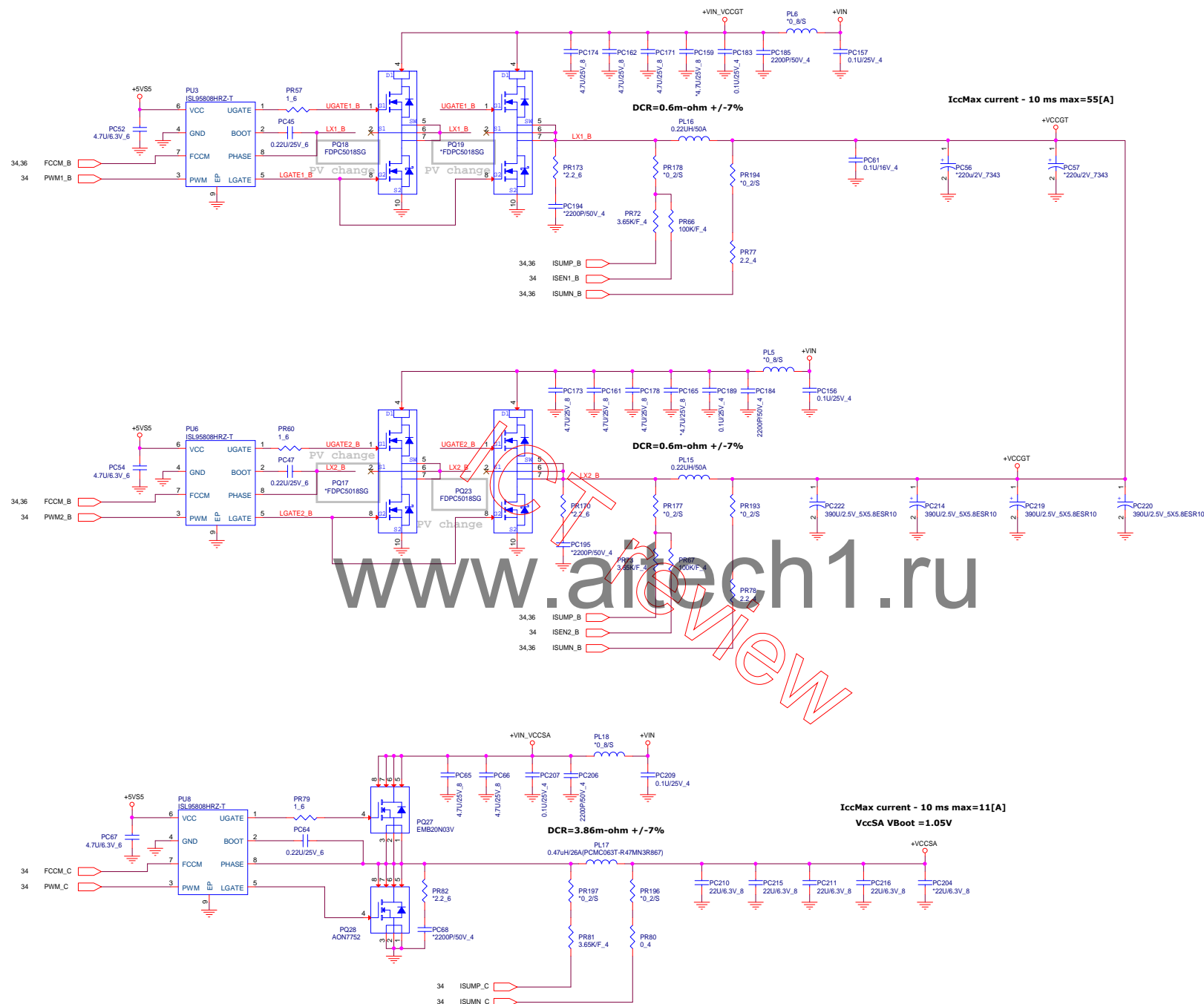
+VIN 20,23,25,27,29,30,31,34,35,36,37  
 +3VS5 10,12,14,16,24,27,28,30,33,37  
 +5VS5 10,22,24,25,30,31,33,34,35,36,37  
 +1.0V\_DEEP\_SUS 10,11,14,16,33













+3V 5,9,10,11,12,13,14,16,17,18,19,20,21,22,23,24,25,26,27,28,34  
 +5V 20,21,22,23,24,25,26,27  
 +3VS5 10,12,14,16,24,27,28,30,33  
 +5VS5 10,22,24,25,30,31,32,33,34,35,36  
 +3VSUS 23,25  
 +3VLANVCC 22

